PCN
Product/Process Change Notification

Capacity extension with 8 inches conversion for Ultrafast diodes production line

Notification number:	ADG-DIS/18/10842	**Issue Date**	04/05/2018
Issued by	Aline Augis		
Product series affected by the change:		200V to 600V Ultrafast diodes ≥ 4A (except SMB/SMC/Axial Packages)	
Type of change: Wafer diameter change		Front end realization	

Description of the change

STMicroelectronics is qualifying an additional Front-End line for ultrafast diodes based on **8 inch** (200mm) wafer diameter.

Reason for change

STMicroelectronics has decided to expand the manufacturing capacity of **ultrafast diodes**. This additional wafer fab capacity will be done through **8 inch** production line located in the same current existing plant

This production upgrade is the result of the constant investments made by STMicroelectronics in the technology and the evolution of discrete devices. It illustrates the commitment of the Company to reinforce its **leading position** in the Power Rectifiers market.

With this 8 inch wafer line investment, STMicroelectronics will increase its **production capacity** to better serve its customers through service improvement and lead time reduction, especially as volumes grow.

Former versus changed product:	The changed products do not present modified electrical, dimensional or thermal parameters, leaving unchanged the current information published in the product datasheet. The die design and layout remain the same, whatever the wafer size. The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. The footprint recommended by ST remains the same. There is no change in the packing modes and the standard delivery quantities either. The products remain in full compliance with the ST ECOPACK®2 grade (“halogen-free”).

Disposition of former products

As the purpose is a manufacturing capacity extension, shipments will be supported using the two production lines.

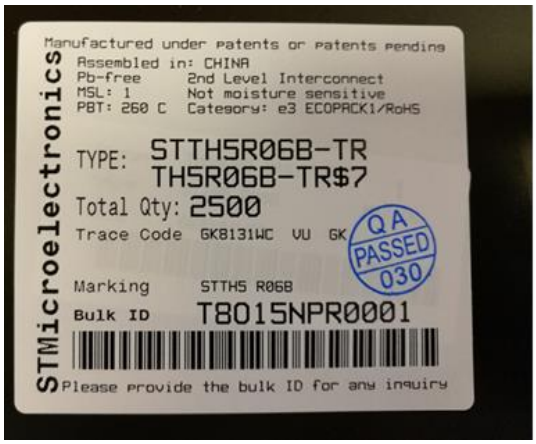
Marking and traceability

New finished good codes created for 8'' products. Examples of FG codes and labels here below:

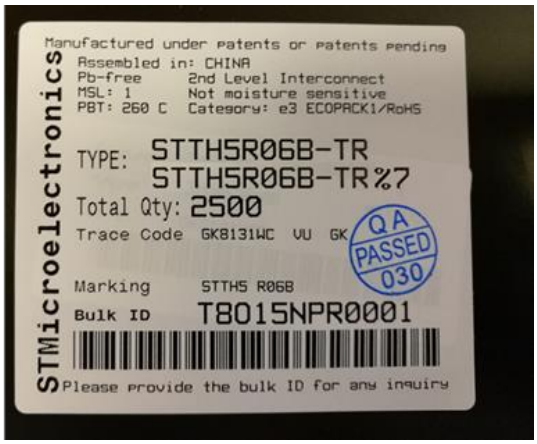
Sales type	6'' Finished Good code	8'' Finished good code
STTH100W06CW	STTH100W06CW-H/7	TH100W06CW$7
STTH15R06D	TH15R06D/7	TH15R06D$7
STTH1002CT	STTH1002CT-H/7	TH1002CT$7
STTH2003CFP	STTH2003CFP/B	TH2003CFP$B

The digit before last will be $ for each 8 inch finished good code.

8'' product label



6'' product label



Qualification complete date	Week 17-2018

Forecasted sample availability

Samples are available on demand.

Change implementation schedule

Sales types	Estimated production start	Estimated first shipments
All	Week 21- 2017	Week 31- 2018

Comments:	

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.

According JEDEC JESD46, absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change. Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change.	
Qualification program and results	QRP18029 Attached

Reliability Evaluation Report

Qualification of Ultrafast diodes
8 inches (200mm) conversion for wafer diameter

General Information	
Product Line	*Rectifiers*
Product Description	*Ultrafast diodes 200V to 600V ≥4A*
Product perimeter	*STTHxx02x* *STTHxx03x* *STTHxx04x* *STTHxx06x*
Product Group	*ADG*
Product division	*ASD&IPAD*
Package	*Multiple (except SMB/SMC/Axial packages)*
Maturity level step	*QUALIFIED*

Locations	
Wafer fab	*ST TOURS - FRANCE*
Assembly plant	*Multiple*
Reliability Lab	*ST TOURS - FRANCE*
Reliability assessment	PASS

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	25-Apr-2018	7	Isabelle BALLON	Julien MICHELON	Initial qualification: Ultrafast diodes 200V to 600V ≥4A in multiple packages except SMB/SMC/Axial packages

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
HTRB	High Temperature Reverse Bias
TC	Temperature Cycling
GD	Generic Data

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify 8inches wafer diameter conversion for Ultrafast diodes 200V to 600V ≥4A assembled in multiple packages except SMB/SMC/Axial packages.

The product series involved in this qualification are listed below.

Product sub-Family	Packages	Product devices
Ultrafast diodes 200V to 600V ≥4A	Multiple packages except SMB/SMC/Axial packages	All STTH 200V to 600V (STTHxx02x – STTHxx03x – STTHxx04x – STTHxx06x)

The reliability test methodology used follows the JESD47-H: « Stress Test Driven Qualification Methodology » The following reliability tests ensuing are:

- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- TC to ensure the mechanical robustness of the products.

Similarity methodology is used. See 5.1 “comments” for more details about similarities.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Change description

No change in terms of electrical, dimensional or thermal performances.
The process key parameters comparison and the different tests have shown that there is no impact on electrical results of the products with the reference to their datasheet.

4.2 Construction Note

	STTHxx02x – STTHxx03x – STTHxx04x – STTHxx06x
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours - FRANCE
Technology / Process family	Ultrafast diodes 200V to 600V ≥4A
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours - FRANCE
Assembly information	
Assembly site	Multiple
Package description	Multiple packages except SMB/SMC/Axial packages
Final testing information	
Testing location	Multiple

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Part Number	Package	Back-End location	Comments
L1	STTH2003CG-TR	D^2PAK	ST Shenzhen (China)	1st Qualification lot - Ultrafast 300V
L2	STTH6002CW	TO-247		2nd Qualification lot – Ultrafast 200V
L3	STTH5R06B-TR	DPAK		3rd Qualification lot - Ultrafast 600V
L4	STTH5R06B-TR	DPAK	Subcontractor A (China)	4th Qualification lot – Ultrafast 600V
L5	STTH6003CW	TO-247	Subcontractor B (China)	5th Qualification lot – Ultrafast 300V
L6	STTH6006W	DO-247	ST Shenzhen (China)	6th Qualification lot – Ultrafast 600V

Detailed results in below chapter will refer to these references.

5.2 Test plan and results summary

Test	Std ref.	Test conditions	SS total	Steps / duration	Failure/SS					
					L1	L2	L3	L4	L5	L6
Die Oriented										
HTRB	MIL-STD-750-1 M1038 Method.A	VR = 80%VRRM Tj =150°C	385	1Khrs	0/77	0/77	0/77		0/77	0/77
Package Oriented										
TC	JESD22 A-104	-65/+150°C 2 cy/h	308	500cy	0/77	0/77		0/77	0/77	
				1Kcy	0/77	0/77		0/77	0/77	

6 ANNEXES

6.1 Tests description

Test name	Description	Purpose
Die-oriented		
HTRB High Temperature Reverse Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package-oriented		
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.